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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/810,105	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5-7, 9-11, 14-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al. (US Pat. 5976912) in view of Moden (US Pat. 6310390).

Regarding claim 1, Fukutomi et al. disclose a semiconductor device comprising:

- a plurality of conductive paths/patterns (63/64, central die pad/support region and 69 in Fig. 22g) being formed using photoresist patterning and etching of a metal layer/foil such as copper (Fig. 22a-22c; Col. 22, line 33; Col. 23, lines 5-15), the conductive paths/patterns being electrically separated from one another by a trench (66 in Fig. 22a-g)
- a semiconductor chip (65 in Fig. 22g) disposed on a first conductive path (central die pad/support region-not numerically referenced in Fig. 22c-22g) of the plurality of conductive paths/patterns, the chip being coupled/directly connected/fixed through a die bonding material (Col. 23, line 40)
- the first conductive path having a die pad shape and a size smaller than that of the rear surface of the chip (Fig. 22c-g)

- a second conductive path/pattern having a bonding pad shape (pattern 64 outside and underneath the chip in Fig. 22a-g) being formed/disposed peripherally around/outside the chip
- the second conductive path/pattern having integral portions outside the chip and underneath the chip (each portion not numerically referenced in Fig. 22c-22g), the portion underneath the chip being formed between the periphery of the chip and the first conductive path, being extended to the rear surface of the chip and coupled/bonded to the chip through a die bonding/adhesive material (66 in Fig. 22c; Col. 23, line 41)
- connecting means such as metallic bonding wires (67 in Fig. 22g) for electrically connecting the chip to the second conductive path, and
    - an insulating resin/epoxy adhesive (68 in Fig. 22c-22g) covering the entire front and rear exposed surfaces of the chip and the die bonding/adhesive material filling in the trench (66 in Fig. 22c-g), the adhesive material integrally supporting the conductive paths with their bottom surfaces being partially exposed

(Fig. 22g; Fig. 22a-g; Col. 22, line 25- Col. 24, line 10).

Fukutomi et al. further teach:

- a third conductive path having a shape of an external connecting pad/terminal (see 61 in Fig. 22g), and
- other embodiments using a variety of bonding material for bonding among a chip, a substrate and conductive patterns/layers where the bonding material includes a silver paste/thermally conductive paste or an insulating tape/adhesive (Col. 9, line 13; Col. 15, lines 13-15 and line 65) between the chip and the die pad.

Fukutomi et al. fail to explicitly teach the third conductive path being coupled/bonded to the chip through an insulating material.

Fukutomi et al. further teach another embodiment (Fig. 17a-g) comprising a plurality of insulating material (36/41 in Fig. 17g) and a plurality of conductive paths (see 33, 42, etc. in Fig. 17a-g) including an insulating adhesive (see 36 in Fig. 17a-g) and an insulating resin (see 41 in Fig. 17a-g) between the chip and the wiring pattern/third conductive path to provide the desired bonding and rigidity (Col. 16, line 15- Col. 17, line 40).

Moden teaches a different configuration of conductive paths/conductors having bonding pad shape and being bonded/coupled with a chip through an insulating material (14/28, 12 and 36/18 respectively in Fig. 1C) where the chip being is disposed on a plurality of conductive patterns (14B, 14A/40A, 40B, etc. in Fig. 1E; Fig. 1A-1E) having different width dimensions to provide an increased density of bonding pads (Col. 4, lines 15-20) where conductive pattern/paths (14A/40A and 28 respectively in Fig. 1E) are bonded/coupled to the chip through insulating material including a polyimide tape and the encapsulating resin (see 36 and 18 in Fig. 1C; Col. 3, line 30- Col. 4, line 50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the third conductive path being coupled/bonded to the chip through an insulating material as taught by the embodiments of Fukutomi et al. and Moden so that the bonding pad density/wiring layout can be improved and the shorting defects can be reduced in Fukutomi et al's device.

Regarding claim 2, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, except the third conductive path having a larger size than that of the second conductive path.

Moden further teaches the third conductive path having a larger width dimension than that of the second conductive path (see width dimensions of 28 versus 40A in Fig. 1E; Col. 4, lines 1-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the third conductive path having a larger size than that of the second conductive path as taught by Moden so that the bonding pad density/wiring layout can be improved and the shorting defects can be reduced in Fukutomi et al's device.

Regarding claim 5, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 1 and 2 above, wherein Fukutomi et al. teach the insulating material such as an insulating adhesive/epoxy resin between the chip and the wiring patterns/conductive paths which are extended to the rear surface of the chip and the chip (see resin 68 between 65 and 64 in Fig. 22e-g; Col. 23, lines 40- 65).

Regarding claim 6, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 1 and 5 above, wherein Fukutomi et al. teach the insulating material including the resin/epoxy adhesive and bonding tape/adhesive (68 and 66 respectively in Fig. 22c-22g; see Col. 15, lines 11-15) being provided over the entire region of front and rear surfaces of the chip.

Regarding claim 7, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, wherein Fukutomi et al. teach the connecting means being metallic wires (67 in Fig. 22g).

Regarding claim 9, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, wherein Fukutomi et al. teach the conductive paths being made of the conductive foil/sheet of copper (Col. 22, line 33; Col. 23 lines 1-15).

Regarding claims 10 and 11, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, and Fukutomi et al. further teach an upper surface of the conductive path (64 in Fig. 22a-g) being selectively covered/patterned with a different metallic material/film such as nickel and gold (Col. 23, line 28).

Regarding claim 14, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, wherein Fukutomi et al. teach the insulating material such as an epoxy adhesive/resin being embedded in the trenches between the conductive paths, covering the chip and integrally supporting the conductive paths (see 68 in Fig. 22g; Col. 23, lines 40-50), and a plurality of the second conductive path/another patterns being extended underneath the chip (see pattern 64 outside and underneath the chip) to form the external terminals (see 70 in Fig. 22g; Col. 23, lines 50-60).

Regarding claim 15, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 14 and 1 above, wherein Fukutomi et al. teach the chip being connected to the second conductive path through the metallic bonding wires (67 in Fig. 22g).

Regarding claim 16, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 14 and 1 above, wherein Fukutomi et al. teach the chip being directly connected to the first conductive path (central die pad/support region-not numerically referenced in Fig. 22c-22g).

Regarding claim 17, Fukutomi et al. disclose a semiconductor device comprising:

- a plurality of conductive paths/patterns (63/64, central die pad/support region and 61 in Fig. 22g) being formed using photoresist patterning and etching of a metal layer/foil such as copper (Fig. 22a-22c; Col. 22, line 33; Col. 23, lines 5-15), the conductive paths/patterns being electrically separated from one another by a trench (see 66 in Fig. 22a-g)
- a semiconductor chip (65 in Fig. 22g) disposed on a first conductive path (central die pad/support region-not numerically referenced in Fig. 22c-22g) of the plurality of conductive paths/patterns, the chip being coupled/directly connected/fixed through a die bonding material (Col. 23, line 40)

- the first conductive path having a die pad shape being disposed below and substantially at a center of the chip and a size smaller than that of the rear surface of the chip (Fig. 22c-g)
- a second conductive path/pattern having a bonding pad shape (pattern 64 outside and underneath the chip in Fig. 22a-g) being formed/disposed peripherally around/outside the chip
- the second conductive path/pattern having integral portions outside the chip and underneath the chip (each portion not numerically referenced in Fig. 22c-22g), the portion underneath the chip being formed between the periphery of the chip and the first conductive path, being extended to the rear surface of the chip and coupled/bonded to the chip through a die bonding/adhesive material (66 in Fig. 22c; Col. 23, line 41)
- connecting means such as metallic bonding wires (67 in Fig. 22g) for electrically connecting the chip to the second conductive path, and
- an insulating resin/epoxy adhesive (68 in Fig. 22c-22g) covering the entire front and rear surfaces of the chip and the die bonding/adhesive material filling in the trench (66 in Fig. 22c-g), the adhesive material integrally supporting the conductive paths with their bottom surfaces being partially exposed

(Fig. 22g; Fig. 22a-g; Col. 22, line 25- Col. 24, line 10).

Fukutomi et al. further teach:

- an external connecting shape path/third conductive path having a shape of an external connecting pad/terminal (see 61 in Fig. 22g) disposed below the chip, and

- other embodiments using a variety of bonding material for bonding among a chip, a substrate and conductive patterns/layers where the bonding material includes a silver paste/thermally conductive paste or an insulating tape/adhesive (Col. 9, line 13; Col. 15, lines 13-15 and line 65) between the chip and the die pad.

Fukutomi et al. fail to explicitly teach the external connecting shape path being coupled/bonded to the chip through an insulating material.

Fukutomi et al. further teach another embodiment (Fig. 17a-g) comprising a plurality of insulating material (36/41 in Fig. 17g) and a plurality of conductive paths (see 33, 42, etc. in Fig. 17a-g) including an insulating adhesive (see 36 in Fig. 17a-g) and an insulating resin (see 41 in Fig. 17a-g) between the chip and the wiring pattern/third conductive path to provide the desired bonding and rigidity (Col. 16, line 15- Col. 17, line 40).

Moden teaches a different configuration of conductive paths/conductors having bonding pad shape and being bonded/coupled with a chip through an insulating material (14/28, 12 and 36/18 respectively in Fig. 1C) where the chip being is disposed on a plurality of conductive patterns (14B, 14A/40A, 40B, etc. in Fig. 1E; Fig. 1A-1E) having different width dimensions to provide an increased density of bonding pads (Col. 4, lines 15-20) where conductive pattern/paths (14A/40A and 28 respectively in Fig. 1E) are bonded/coupled to the chip through insulating material including a polyimide tape and the encapsulating resin (see 36 and 18 in Fig. 1C; Col. 3, line 30- Col. 4, line 50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the external connecting shape path being

coupled/bonded to the chip through an insulating material as taught by the embodiments of Fukutomi et al. and Moden so that the bonding pad density/wiring layout can be improved and the shorting defects can be reduced in Fukutomi et al's device.

Regarding claim 18, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 17 above, wherein Fukutomi et al. teach the connecting means such as metallic wires (67 in Fig. 22g) for electrically connecting the chip to the bonding pad shaped conductive path.

Regarding claim 19, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 17 above, wherein Fukutomi et al. teach the insulating material such as an epoxy adhesive/resin being embedded in the trenches between the conductive paths, covering the chip and integrally supporting the conductive paths (see 66/68 in Fig. 22c-22g).

Regarding claim 20, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 17 above, except the external connecting shape conductive path having a larger size than that of the conductive path of the die pad shape.

Moden further teaches the third conductive/external connection path having a larger width dimension than that of the second conductive path (see width dimensions of 28 versus 40A in Fig. 1E; Col. 4, lines 1-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the conductive path of the external connecting shape having a larger size than that of the conductive path of the die pad shape as taught by Moden so that the bonding pad density/wiring layout can be improved and the shorting defects can be reduced in Fukutomi et al's device.

Regarding claim 21, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 17 and 20 above, wherein Fukutomi et al. teach the insulating material such as an insulating adhesive/epoxy resin between the chip and the wiring patterns/conductive paths which are extended to the rear surface of the chip and between the external connecting shaped conductive path and the chip (see 66 in Fig. 22c-22g).

Regarding claim 23, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 17 above, and Fukutomi et al. further teach an upper surface of the conductive paths (64 in Fig. 22a-g) being selectively covered/patterned with a metallic material/film such as nickel and gold (Col. 23, line 28).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al. (US Pat. 5976912) and Moden (US Pat. 6310390) as applied to claim 1 above, and further in view of admitted prior art (APA).

Regarding claim 3, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claim 1 above, except the second conductive path being in a form of an island.

APA teaches a conventional package structure having a wiring configuration comprising a plurality of conductive paths (51, 53, 54, etc, in Fig. 10A) where a second conductive path includes a bonding pad in a shape of an island (53 in Fig. 10A; specification pages 1 and 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the second conductive path being shaped in the form of an island as taught by APA so that the desired electrical resistance can be achieved and wire bonding /repair can be improved in Moden and Fukutomi et al's device.

4. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al. (US Pat. 5976912), Moden (US Pat. 6310390) and APA as applied to claims 1 and 3 above, and further in view of Hansford (US Pat. 6211575).

Regarding claim 13, Fukutomi et al., Moden and APA teach substantially the entire claimed structure as applied to claims 1 and 3 above, except the second conductive path formed in the island being a test pin.

Hansford teaches an integrated circuit (IC) package structure where a circuit testing and circuit identification for a die and the package is performed using conventional connections including bonding pads and testing pins (Col. 1, lines 25-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive island of the second conductive path

as a test pin as taught by Hansford so that the electrical/reliability testing and rework capability can be improved in APA, Moden and Fukutomi et al's device.

5. Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al. (US Pat. 5976912) and Moden (US Pat. 6310390) as applied to claims 1 and 17 respectively above, and further in view of Fjelstad (US Pat. 6001671).

Regarding claims 8 and 22, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 1 and 17 respectively above, except the side of each of the conductive paths being curved to mate with the insulating resin.

Fjelstad teaches forming curved sides of conductive wiring/paths mating with the insulating resin (Fig. 7E-7G; Col. 8) to improve the resin adhesion and bonding.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the side of each of the conductive paths being curved to mate with the insulating resin as taught by Fjelstad so that the resin adhesion and bonding can be improved in Moden and Fukutomi et al's device.

6. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukutomi et al. (US Pat. 5976912) and Moden (US Pat. 6310390) as applied to claims 1 and 17 respectively above, and further in view of Kweon et al. (US Pat. 5900676).

Regarding claims 12 and 24, Fukutomi et al. and Moden teach substantially the entire claimed structure as applied to claims 1 and 17 respectively above, except the first conductive path or the die pad shaped conductive path of the die pad shape being coupled with a conductive pattern on a mounting board through a thermally conductive material.

Kweon et al. teach mounting/coupling of a device on a printed circuit board (PCB)/mounting board (140 and 300 respectively in Fig. 14) where a die pad/first conductive path is coupled to a conductive/thermally dissipative pattern on the PCB/mounting board (150 and 312 respectively in Fig. 14; Col. 7, line 1-20) through a solder plated/thermally conductive material (150 in Fig. 13-15).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to couple the first conductive path with a conductive pattern formed on the mounting board through a thermally conductive material as taught by Kweon et al. so that heat dissipation and bonding can be improved Moden and Fukutomi et al's device.

Response to Arguments

7. Applicant's arguments filed on 01-23-04 have been fully considered but they are not persuasive.

A. Applicant contends that Fukutomi et al. and Moden do not teach the another path/third path being coupled to the chip through the insulating material.

However, as explained above, Fukutomi et al. teach a variety of configurations comprising a plurality of insulating material and a plurality of conductive paths including the embodiment (Fig. 17a-g) having the plurality of insulating material (36/41 in Fig. 17g) and the plurality of conductive paths (see 33, 42, etc. in Fig. 17a-g) where the insulating adhesive (see 36 in Fig. 17a-g) and the insulating resin (see 41 in Fig. 17a-g) is disposed between the chip and the wiring pattern/third conductive path to provide the desired bonding and rigidity (Col. 16, line 15- Col. 17, line 40).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

Nitin Parekh

NP

04-06-04

[illegible]er

Steven Loke